PC-based Real-time Power-system Simulation Takes an Effective Step Forward

by Christian Dufour, Jean Bélanger and Simon Abourida of Opal-RT Technologies Inc., Montreal, QC, and Paul Baracos of ACS Enrg., Montreal, QC

Abstract

In the Summer 2001 issue of the IEEE Canadian Review, Lechevin, Rabbath and Baracos reported on distributed real-time simulation of power systems using off-the-shelf software. Since then, improvements in the ARTEMIS solver now allow a significant reduction in numeric error for a given integration step size in switching networks. The innovation comes from implementing an interpolation mechanism that accurately takes into account between-step switching events. This means that a given system can be simulated at a relatively large step size, but with the same accuracy as if a smaller, and more computationally intensive, step size had been used. By interpolating between time steps, the algorithm gives a smaller effective step size for greater integration accuracy.

This paper shows how the new algorithm improves the accuracy of a six-pulse-inverter simulation and discusses a number of possible applications involving electric drives and power converters.

Sommaire

Dans l'édition "Été 2001" de La revue canadienne de l'IEEE, Lechevin, Rabbath et Baracos ont discuté de méthodes de simulation en temps-réel de réseaux électriques utilisant des ordinateurs non-spécialisés disponibles commercialement. Depuis, des améliorations au programme ARTEMIS permettent une encore plus grande précision de simulation dans les systèmes électrique comprenant des commutateurs. L'innovation vient de l'implantation d'un mécanisme d'interpolation permettant de prendre en compte précisément les commutations qui se produisent entre les pas de calcul. Cela permet de simuler un système électrique à un pas de calcul beaucoup plus grand que sans interpolation, tout en conservant une précision équi-valente. En interpolant entre les pas de calcul, l'algorithme a donc un pas de calcul effectif plus petit et donc une précision de calcul plus grande.

Cet article montre comment le nouvel algorithme améliore la précision de simulation en temps-réel d'un onduleur triphasé. L'article discute aussi de quelques autres applications possibles, tels que convertisseurs de puissance et circuits d'alimentation de machines électriques.

1.0 Introduction

In the Summer 2001 issue of the IEEE Canadian Review [1], Lechevin, Rabbath and Baracos reported on distributed real-time simulation of power systems using off-the-shelf software with the Advanced Real-Time Electro-Mechanical Transient Simulator (ARTEMIS) algorithm. Whereas conventional system simulation tools [3,6] use the Tustin, or trapezoidal, discretization method, whose drawbacks include undamped switching oscillations and poor discretization of discrete components near the Nyquist limit, ARTEMIS' proprietary discretization methods [1] often can reduce numeric oscillation and improve discretization. The result is oscillation-free simulation of switching energy systems, without needing snubbers or other stabilizing schemes [4], and greater accuracy in circuits containing slightly damped components, which the well-known trapezoidal method sometimes handles inadequately.

However, as with other fixed-time-step-capable simulation software like EMTP [2] and SimPowerSystems (formerly known as the Simulink Power System Blockset) [6], the standard ARTEMIS software cannot precisely simulate circuits that contain switches that toggle in the middle of time-steps. This is due to the non-iterative integration algorithm of these software packages, in which changes in network topology can only be taken into account at the beginning of the time-step. Events that occur in the middle of the time-step can only take effect at the following time-step. In the case of systems that include switching components such as thyristors and GTO converters, this variable discrete switching latency distorts the output spectrum of the simulation by introducing low frequency jitter components. This jitter is introduced by the simulation method and is not a real phenomenon.

To solve this problem we have developed an extension of the ARTEMIS algorithm to allow Real Time compensation of between-step switching Events (ARTEMIS-RTE). This algorithm can give very significant improvements in numeric accuracy with only a small increase in computational overhead, typically less than 10% of the real-time step. It can therefore be used in real-time applications with negligible increase in the computational costs.

This paper compares of accuracy of conventional and compensated fixed-time-step simulations of switched systems Section 2.0 describes the jitter problem encountered in the fixed-time-step simulation of a simple thyristor converter. Section 3.0 demonstrates the use of the ARTEMIS-RTE algorithm in the single thyristor converter while Section 4.0 does the same for a multi-switch system, a three-phase inverter. Section 5.0 briefly describes the RT-Event blockset used to design event-compensated controls. Finally, conclusions are put forward in Section 6.0.

2.0 Jitter: an Artifact of Fixed-Time-Step Simulation

Standard fixed-time-step simulation of cyclically switched circuits often leads to numerically induced jitter in the simulation outputs. This jitter is purely an artifact of the numeric simulation process - it is absent from the real system or even from a variable-time-step simulated system, which can therefore serve as a reference.

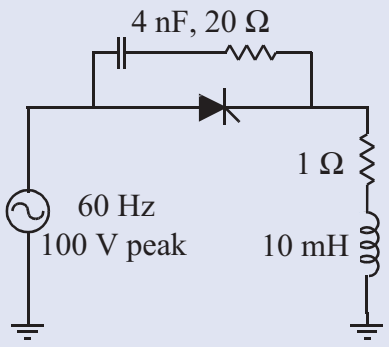

Figure 1: A single-phase thyristor converter.

Very simple switching circuit simulations can exhibit numerically induced jitter. The simple thyristor converter illustrated in Figure 1 is an example. Suppose that the thyristor is activated with a constant firing angle θ. In fixed-step simulation, θ is rounded to the next time-step hit. As a result, the fixed-step simulation output exhibits a jitter that is absent from the reference simulation, as shown for θ=120° and Ts=50 μs in Figures 2 and 3.

3.0 ARTEMIS-RTE Real-Time Event Compensation

An interpolation-extrapolation algorithm has been implemented in ARTEMIS-RTE to compensate for switching events that occur in the middle of fixed-time-steps. When a switching discontinuity is detected, states are interpolated for the fraction of the step detected. After the dis-

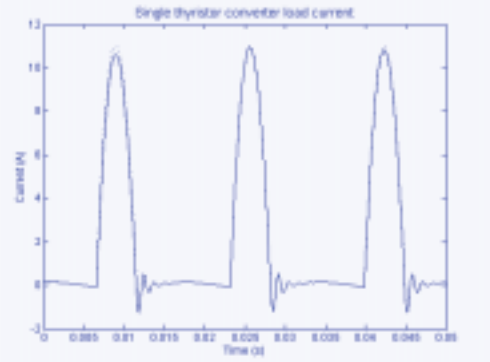

Figure 2: Thyristor converter: simulated load current.

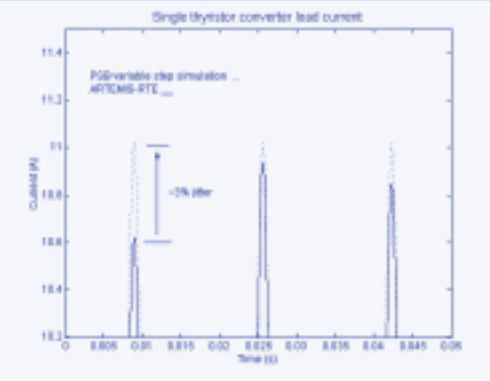

Figure 3: Detail of the load current showing the jitter.

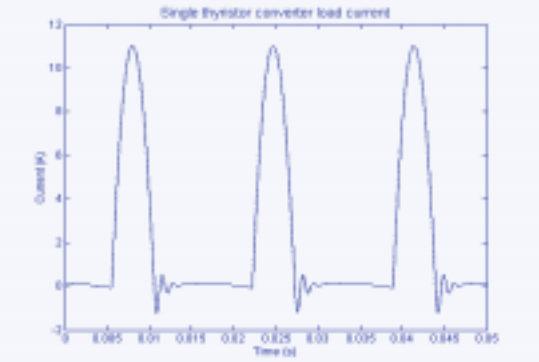

Figure 4: ARTEMIS-RTE simulation of the thyristor circuit's load current.

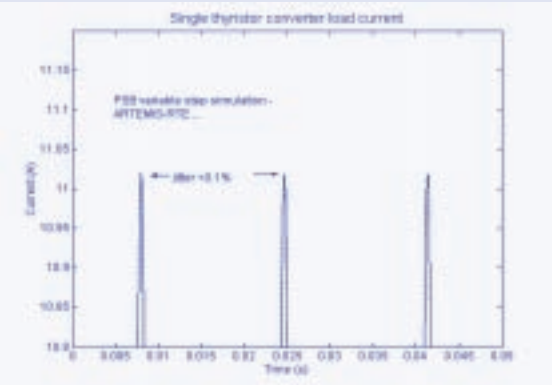

Figure 5: ARTEMIS-RTE simulation output detail showing reduced jitter.

continuity has been interpolated, a normal iteration is made, followed by an extrapolation to resynchronize the simulation with the next fixed time-step frame.

The ARTEMIS-RTE simulation of the simple thyristor circuit from Figure 1 is shown in Figures 4 and 5.

The conventional fixed-step simulation's 3% jitter, measured at the peak values of load current, has come down to less than 0.1% with ARTEMIS-RTE. Both simulations used a time-step of 50µs. Clearly, the ARTEMIS-RTE simulation output is more accurate in both peak and average levels.

The effect of the ARTEMIS-RTE algorithm can also be noted in the frequency spectrum, through the use of Discrete Fourier Transform. Figure 6 show the jitter improvement for the thyristor converter for a time-step of 60µs.

4.0 Simulation case: DC-AC inverter

The simulated circuit schematic is shown in Figure 7. It is a DC-AC inverter composed of a DC source feeding a six-pulse IGBT bridge, a three-phase transformer and a R-C load. Simulation is carried out in open loop and the firing control is a standard PWM scheme. The circuit has 12 states, 13 inputs, 14 outputs and 6 switches.

This circuit is especially difficult to accurately simulate in fixed time step because of the occurrences of multiple switching events in a single step. The ARTEMIS-RTE algorithm deals well with this type of circuits with no extra computational time, as compared with the single-event case.

The simulation of this circuit with standard SimPowerSystems at a real-time compatible time step of 50 µs is shown in Figure 8. Output voltage is noisy and inaccurate, mainly because PWM switching scheme involves very-high and precise switching sequences that a standard non-iterative simulation algorithm cannot follow.

In contrast, the ARTEMIS-RTE algorithm deals well with this kind of switching patterns, dividing Total Harmonic Distortion (THD) by a factor of three. Those patterns include multiple switching in a single time-step and instantaneous switching of diodes.

4.1 Linearity of the DC-AC inverter

The linearity of the voltage output versus the modulation index input is shown in Figure 9. As can be seen in the figure, the ARTEMIS-RTE simulation is linear as opposed to the general Tustin case. The Tustin method of SimPowerSystems works well only when the time step size is an exact sub-multiple of both output period and PWM period. For 60 Hz output and 1080 Hz PWM frequency, this happens only for time steps calculated as shown below:

Step size (seconds) = 1/(60*1080*n), for $n \in 1, 2, 3 \ldots$)

These exact time steps of 15.432 µs, 7.716 µs, 5.144 µs, …, are unattainable using current PC technology. At the more practical time step size of 50 µs, not a sub-multiple of output and PWM frequencies, the ARTEMIS-RTE algorithm exhibits excellent linearity while the Tustin shows some non-linearity. The two curves in Figure 9 show the maximum and minimum values of the measured fundamental generated using the Tustin method with a 50 µs time step, because this value is subject to jitter.

4.2 Achievable step size versus PWM frequency.

The non-iterative nature of the ARTEMIS-RTE algorithm typically causes a minor increase of both average and real-time simulation step times when compared to the uncompensated case. This non-iterative method has some limitations with regards to the frequency of switching in the simulation. Nevertheless, the ARTEMIS-RTE works well at time steps achievable in real-time applications with a switching scheme like the PWM converter of Figure 7.

As seen in Figure 10, the ARTEMIS-RTE algorithm can keep minimal error (<1%) at time steps compatible with real-time implementation. In contrast, the Tustin method is not designed to handle discrete-switching events occurring in PWM schemes at large time step sizes.

For a 2 kHz PWM carrier frequency, a 47 µs ARTEMIS-RTE simulation has an effective time step of 2 µs, meaning that one would have to lower the time step size to 2 µs in a regular uncompensated simulation

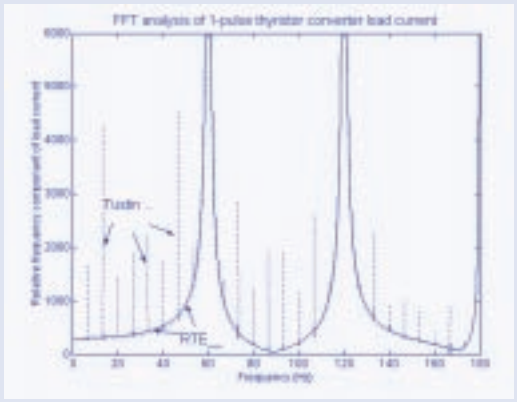

Figure 6: Frequency spectrum of the thyristor controller's load current: ARTEMIS-RTE vs. uncompensated Tustin method.

to obtain the same accuracy as an ARTEMIS-RTE simulation at 47 µs.

4.3 Achievable real-time step size.

RT-LAB software from Opal-RT Technologies is a real-time application software that enables simulation of Simulink-RTW schematics on a variety of low-cost target platforms, either single-processor or multi-processor Pentium-class machines such as the three-processor unit shown in Figure 11. The unit shown is slated for delivery to vehicle manufacturer who will use it to test thyristor and IGBT based motor drive controllers. Similar simulators have been delivered to train manufacturers.

Table 1: Computation times for PWM Inverter (Pentium III, 1GHz)

	ARTEMIS-RTE
Average time step	12 µs
Real-time step	14 µs

Including processor communication time overhead brings the minimum achievable step size in RT-Lab to 35µs for the PWM inverter. This shows that the PWM inverter can be simulated in real-time within the ARTEMIS-RTE limits of Figure 10.

The real-time performance of ARTEMIS-RTE is due to the fact that the algorithm is always non-iterative, even during the steps that have switch actions. This is in contrast with software with similar capabilities that iterate one or more times during discontinuity-occurring steps [5,7].

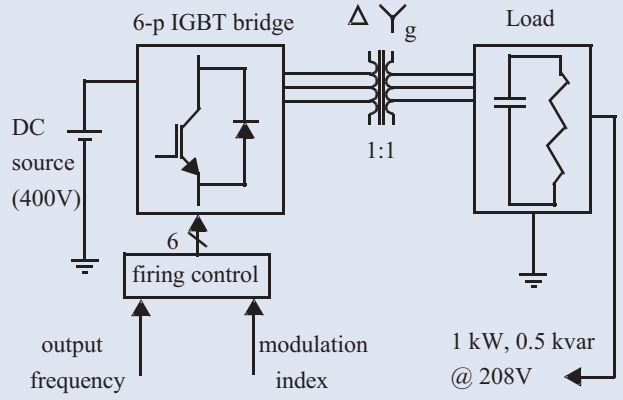

Figure 7: PWM inverter schematic

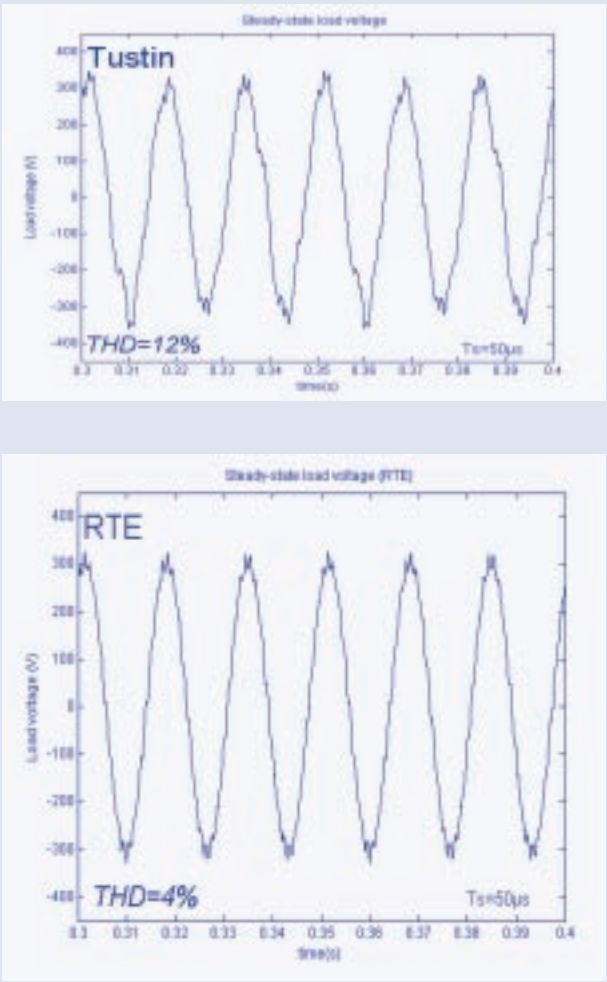

Figure 8: PWM simulation results.

The ARTEMIS-RTE algorithm is commercially available as an add-on to the popular Simulink/SimPowerSystems package or as an integral part of the RT-LAB Electric Drive Simulator which is a table-top simulation device that provides a low-risk, low-cost entry point to high-fidelity hardware-in-the-loop real-time modeling and control prototyping using high-speed I/O cards available off-the-shelf from National Instruments. Typical SimPowerSystems models update in less than 50 microseconds with 200 nanosecond gate-firing precision. This performance level can be maintained for larger models by adding processors (up to seven!) in a shared-memory industrial chassis no larger than a standard desktop computer.

Typical applications include controllers and simulators for electric drives, electric vehicles, gas-turbine generator sets, wind turbines and small to medium-sized electric systems of all sorts.

5.0 Applying between-step event compensation to control block diagram

The ARTEMIS-RTE algorithm applies between-step event compensation to electric systems modeled with SimPowerSystems, but it is not applicable to the remaining subsystems of a Simulink block diagram such as the control subsystems. When between-step events cause numeric problems in control subsystems, compensation can be introduced manually using the RT-Events toolbox. This was the case with PWM inverter of Figure 7. The RT-Events toolbox contains a number of standard blocks, such as comparators and integrators, which are used to replace corresponding blocks from the standard Simulink libraries. In other respects, the block diagram is unmodified, as shown in Figure 12.

The RT-Event blocks have the same functionality as their Simulink counterparts except that they output additional timing information on

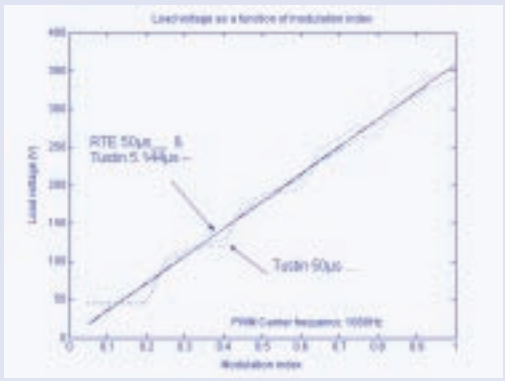

Figure 9: PWM inverter linearity.

between-step events such as zero-crossings. The RT-Events blockset has already been successfully used by Ford Motor to model internal combustion engine and is detailed in [8].

6.0 Conclusion

This article highlights a novel algorithm called Real Time compensation of switching Events. This algorithm allows a more accurate fixed-step simulation of time-segment linear dynamic systems with switching events that occur in the middle of time-steps.

Some simple simulation cases have been discussed, to show the increased precision of the algorithm. The cases presented exhibited output jitter when not compensated, a common problem arising in the fixed-step simulation of electrical systems containing non-linear components like switches.

The discrete simulation of a DC-AC inverter with ARTEMIS-RTE has shows that it results in a small signal linear characteristic for the inverter in fixed time step. This characteristic is obtained at time steps compatible with real-time implementation and thus makes the software ideal for discrete control or HIL applications.

It has been shown that this algorithm has dramatically reduced simulation jitter in the presented cases, with very small computational overhead in all cases. This overhead, even in single-step multi-event cases, represents less than 10% of the normal ARTEMIS state-space iteration routine.

The ARTEMIS-RTE algorithm is currently implemented in the ARTEMIS Add-On for the Power System Blockset for Simulink, but can be adapted to other simulation packages.

Suggested application areas include controllers and simulators for electric drives, electric vehicles, gas-turbine generator sets, wind turbines and small to medium-sized electric systems of all sorts.

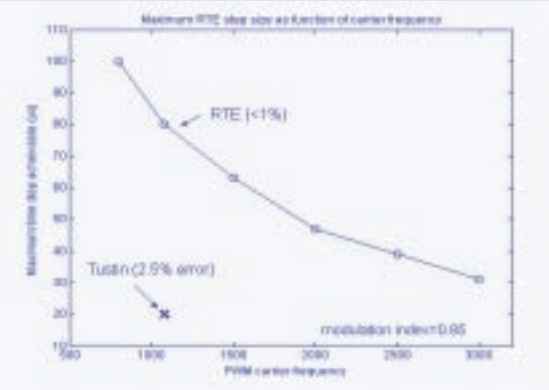

Figure 10: Maximum ARTEMIS-RTE time step for 1% error in the fundamental component amplitude vs. PWM frequency.

Figure 11: Multi-processor Electrical Engineering Simulator, an industrial-quality unit equipped with three 1 GHz CPUs (expandable to 5 by adding one dual-CPU board). The CPUs communicate via shared memory, and multiple units can be linked via FireWire to assemble a mega-simulator.

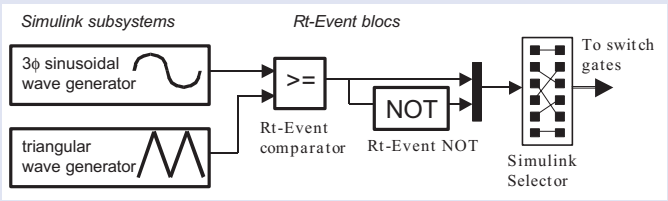

Figure12: RT-Events PWM controller

7.0 Acknowledgments

The compensation algorithm of ARTEMIS has been developed under a National Science and Engineering Research Council industrial research grant. The authors would also like to thank Nicolas Léchevin, Biao Yu and Vincent Lapointe.

8.0 References

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About the authors

Christian Dufour is a Simulation Software Specialist at Opal-RT Technologies. He received his Ph.D. degree from Laval University, Quebec in 2000. Since 1992, he has worked in the development of IREQ real-time simulator as well as The MathWorks' Power System Blockset. His current research interests are mainly focused on numerical techniques related to real-time power system simulations.

Simon Abourida has a Masters degree in electrical engineering from École Polytechnique, with specialization in power systems and power electronics (1994). He has worked for Hydro-Quebec's International Real-Time Power System Simulator, and at Technologies M4. He is now with Opal-RT Technologies as the Electromechanical Modeling & Simulation Group Leader where he is involved in the design and testing of real-time digital simulators and other related real-time applications.

Jean Belanger is president of Opal-RT Technologies, Inc. He is a specialist in real-time simulations, with more than 20 years of experience in the field, including many years as part of the simulation division of Hy-dro-Quebec. He received his M.A.Sc. from Laval University, Quebec, and is a member of the Order of Professional Engineers of Quebec.

Paul Baracos has been involved in simulation and control systems since 1976. He has a B.Sc. in Physics from the University of Manitoba, an M.A.Sc from Systems Design Engineering from the University of Waterloo and a Ph.D. in Mechanical Engineering from McGill University. He has had twenty-years experience as professional engineers, and is currently president of ACS Enrg., a registered consulting and software company.

Letters to the Managing Editor / *Lettres envoyées au rédacteur en chef*

Obituary

Michel Lecours - Engineering educator

Michel Lecours, Fellow member, died 21 October. He was 62 years old.

Mr. Lecours graduated from École Polytechnique, Montréal, Canada, in 1963, and received his Ph.D. degree in electronics and communications from the Imperial College, London, England, in 1967. From 1967 to 2001, he was a Professor in the Electrical Engineering Department, Laval University, Quebec City, Canada. He was Head of the Electrical Engineering Department, Laval University, from 1975 to 1977, and Vice-Dean of the Faculty of Science and Engineering from 1977 to 1985. He was involved in transmission system engineering at Bell Northern Research, Ottawa, Canada, and was a Visiting Research Scientist in the Digital Mobile Radio Section, Electrical Communication Laboratories, NTT, Yokosuka, Japan. His research interests were in the field of mobile and wireless radio channels, microstrip antenna arrays for mobile communications and radar, and applications of data fusion to identity information expert systems. In the field of technology transfer, he collaborated with Lab-Volt Ltd., Quebec City, Canada, in the development of telecommunication, microwave, radar, and antenna training equipment.

He was Editor of the Canadian Journal of Electrical and Computer Engineering from 1992 to 1998 and served on the executive committee of IEEE Canada (Region 7) from 1995 to 1997. He was the recipient of the 1987 Annual Merit Award presented by the École Polytechnique of Montreal Alumni Association, the 1997 John B. Stirling Medal of the Engineering Institute of Canada, and the 1997 IEEE Regional Activities Board Larry K. Wilson Transnational Award.

He is survived by his wife, three children and two grandchildren.

CR40 - Spring editorial - Income Tax Software

Vijay,

You made an excellent point about the cost of acquiring the software to do your own income tax when the government (CCRA) should provide each taxpayer upon request with the software. However, it is not necessary for them to send a disk as it could be downloaded from a secure site using the SIN number of the taxpayer to access their site. One would then complete the forms and send them back to the CCRA site. This would be cheaper for all. I find that preparing my information and then having my tax accountant fill the form that he gets from CCRA is the cheapest but that is still $50.00 plus GST. The advantage of this approach is that one does not have to supply the receipts and T-slips. **We should all send this suggestion to the Minister responsible for the CCRA and our MP's.**

Harvey Buckmaster

BC.

Vijay

Thank you for your continued efforts in publishing the IEEE Canadian Review.

I always seem to find an interesting article that causes me to read through the entire publication. I was very impressed with Dr. Luchien Chang's article on Wind Energy Conversions Systems (Spring 2002 Publication) as I had some exposure to Dr. Chang's research when he first began and it was interesting to read how his research has progressed. Thank you again for ensuring that we have interesting articles in the Canadian Review.

Stephen A. Galbraith

Ottawa, ON

Editor's note:

We do appreciate your feedback. Thanks.

Subject: Investment tips

If you had bought $1000.00 worth of Nortel stock one year ago, it would now be worth $49.00.

With Enron, you would have $16.50 of the original $1,000.00.

With Worldcom, you would have less than $5.00 left.

If you had bought $1,000.00 worth of Molson (the beer, Stupid, not the stock) one year ago, drank all the beer, then turned in the cans for the 10 cent deposit, you would have $214.00.

Based on the above, my current investment advice is to drink heavily and recycle.

Ann McLoud

Toronto, ON

ps: Valuations may fluctuate with the time/day of the week, but you get the drift. Readers should note that drinking may be harmful to your health; ... to say nothing of investing in the stock market. However, recycling is most definitely recommended.

Editor's note:

The views expressed are the sole responsibility of the author(s). The editor does not condone or support any investment advice received from readers. The mentioning of corporate entities does not mean that such corporations are recommended or otherwise.